Solutions - Homework 4

(Due date: November 20th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

- Using the HCS12D PWM Module, write a C program (*provide a printout*) to generate a 24 KHz signal with a 30% duty cycle on PP5. E-clock = 24 MHz. Indicate the period of the clock source of PWM5.

Example: PWM5 (PP5), 30% Duty Cycle, 24 KHz, E-clock = 24 MHz

Pre-scale factor for Clock A = 4 (not the only possible value): $PWM5\ clock = \frac{24\ MHz}{4} = 6MHz \rightarrow Period = \frac{1}{6}us$
PWM5 desired frequency is 24 KHz $\rightarrow$ $PWM5\ waveform\ period = \frac{1}{24}ms$
To get $\frac{1}{24}ms$ using a base period of $\frac{1}{6}us$, we need $\frac{\frac{1}{24}ms}{1/_6 us} = 250\ cycles$. This is ok since only 8 bits are allowed for period.
For 30% Duty Cycle, we need $250 \times 0.3 = 75$ cycles:

- Select Clock A as the clock source for PWM5: `PWMCLK = 0x00`
- Set clock A prescaler to 4: `PWMPRCLK = 0x02`
- Polarity of PWM5 set to '1': `PWMPOL = 0x20`
- Left aligned mode selected: `PWMCAE = 0x00`
- 8-bit individual PWMs enabled, stop PWM in wait and freeze mode: `PWMCTL = 0x0C`
- Set period value: `PWMPER5 = 250`
- Set duty cycle value: `PWMDTY5 = 75`
- Reset PWM5 counter: `PWMCNT5 = 0x00`
- Enable PWM Channel 5: `PWME = 0x20`

C Code: `hw4p1.c`

PROBLEM 2 (20 PTS)

- HCS12D – SCI1: Complete the following table. E-clock = 24 MHz.

Using the formulas: $Baud\ Rate = Tx\ clock = \frac{E-clock}{16 \times SBR}, Rx\ clock = \frac{E-clock}{SBR}$, we get:

Baud Rate = Tx clock frequency (Hz)	**Rx clock frequency** (Hz)	**SCI1BDH**	**SCI1BDL**
375000	6000000	00	04
1500	24000	03	E8
20000	320000	00	4B
200	3200	1D	4C
500	8000	0B	B8

✓ What are the largest and smallest Baud Rates? Provide the respective values of `SCI1BDH` and `SCI1BDL` on each case.

The largest $SBR = 2^{13} - 1 = 8191 = 0x1FFF$ results in: $Smallest\ Baud\ Rate = \frac{24 \times 10^6}{16 \times 8191} = 183\ Hz$
$\rightarrow SCI1BDH = 0x1F, SCI1BDL = 0xFF$

The smallest $SBR = 1 = 0x0001$ results in: $Largest\ Baud\ Rate = \frac{24 \times 10^6}{16 \times 1} = 1500000\ Hz$
$\rightarrow SCI1BDH = 0x00, SCI1BDL = 0x01$

- HCS12D – SPI0 with the LTC1661 DAC: Using the function `sendLTC1661(char x1, char x2)` found in `unit10a.c`, what are the two pairs of 8-bit values (x1, x2) that should be written in order to have 2.8v on Output B of the DAC (use the datasheet)? Also, if a Baud Rate of 4x10^6 is desired (E-clock=24 MHz), what is the value of `SPI0BR`?

The LTC1661 uses 10 bits to represent incoming digital data:

$$2.8 = \frac{D}{2^{10}} \times 5 \rightarrow D = 573.44$$

We use $D = 573 = 0x23D$, which results in an output voltage of: $\frac{573}{2^{10}} \times 5 = 2.7978v$

Using the LTC1661 datasheet, we need to input the following bitstream:

✓ Control Code: 1010 (Load DAC B, Update Outputs)
✓ Input Code: 10 0011 1101 = 0x23D (10-bit data)
✓ Don't care: 11

This results in: `1010 10 0011 1101 11 = 0xA8F7`

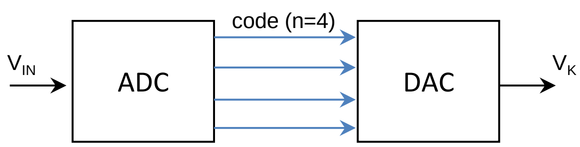
Then, we use: `sendLTC1661(0xA8, 0xF7)` in order to generate 2.8 on Output B of the LTC1661 DAC.

For a Baud Rate of 4x10^6: $BR = 4 \times 10^6 = \frac{24\times10^6}{BR\ divisor} \rightarrow BR\ divisor = 6 = (SPPR+1) \times 2^{(SPR+1)}$

We pick: $SPPR = 2, SPR = 0$. Then: `SPI0BR = 00100000 = 0x20`

PROBLEM 3 (20 PTS)

- Analog to Digital Conversion. Using the successive approximation algorithm with n=4 (codes from `0000` to `1111`), compute the 4-bit codes and the quantized voltages V_k for the following input voltages. V_{DD} = 5v.
  Formula for Quantized voltage: $V_k = \left(\frac{k}{2^n}\right) V_{DD}$



Vin (v)	4-bit code	V_k (v)
4.78	1111	4.6875
0.31	0000	0
2.67	1000	2.5

✓ What is the maximum possible quantization error (in voltage units) with n=4?

Vin = 4.78:

$b_3 = 1 \rightarrow Code = 1000 \rightarrow k = 8 \rightarrow V_k = \left(\frac{8}{2^4}\right)5 = 2.5v \le Vin \rightarrow b_3 = 1$

$b_2 = 1 \rightarrow Code = 1100 \rightarrow k = 12 \rightarrow V_k = \left(\frac{12}{2^4}\right)5 = 3.75v \le Vin \rightarrow b_2 = 1$

$b_1 = 1 \rightarrow Code = 1110 \rightarrow k = 14 \rightarrow V_k = \left(\frac{14}{2^4}\right)5 = 4.375v \le Vin \rightarrow b_1 = 1$

$b_0 = 1 \rightarrow Code = 1111 \rightarrow k = 15 \rightarrow V_k = \left(\frac{15}{2^4}\right)5 = 4.6875v \le Vin \rightarrow b_0 = 1$

$\Rightarrow Code = 1111, V_k = \left(\frac{15}{2^4}\right)5 = 4.6875v$

Vin = 0.31:

$b_3 = 1 \rightarrow Code = 1000 \rightarrow k = 8 \rightarrow V_k = \left(\frac{8}{2^4}\right)5 = 2.5v > Vin \rightarrow b_3 = 0$

$b_2 = 1 \rightarrow Code = 0100 \rightarrow k = 4 \rightarrow V_k = \left(\frac{4}{2^4}\right)5 = 1.25v > Vin \rightarrow b_2 = 0$

$b_1 = 1 \rightarrow Code = 0010 \rightarrow k = 2 \rightarrow V_k = \left(\frac{2}{2^4}\right)5 = 0.625v > Vin \rightarrow b_1 = 0$

$b_0 = 1 \rightarrow Code = 0001 \rightarrow k = 1 \rightarrow V_k = \left(\frac{1}{2^4}\right)5 = 0.3125v > Vin \rightarrow b_0 = 0$

$\Rightarrow Code = 0000, V_k = \left(\frac{0}{2^4}\right)5 = 0v$

Vin = 2.67:

$b_3 = 1 \rightarrow Code = 1000 \rightarrow k = 8 \rightarrow V_k = \left(\frac{8}{2^4}\right)5 = 2.5v \leq Vin \rightarrow b_3 = 1$

$b_2 = 1 \rightarrow Code = 1100 \rightarrow k = 12 \rightarrow V_k = \left(\frac{12}{2^4}\right)5 = 3.75v > Vin \rightarrow b_2 = 0$

$b_1 = 1 \rightarrow Code = 1010 \rightarrow k = 10 \rightarrow V_k = \left(\frac{10}{2^4}\right)5 = 3.125v > Vin \rightarrow b_1 = 0$

$b_0 = 1 \rightarrow Code = 1001 \rightarrow k = 9 \rightarrow V_k = \left(\frac{9}{2^4}\right)5 = 2.8125v > Vin \rightarrow b_0 = 0$

$\Rightarrow Code = 1000, V_k = \left(\frac{8}{2^4}\right)5 = 2.5v$

Maximum Quantization error: This is equal to the equivalent voltage of 1 LSB: $\frac{1}{2^4} \times 5 = 0.3125v$

- HCS12D: For E-clock=24 MHz and n=10, what is the minimum conversion time? Indicate the value of `ADTnCTL4` that achieves this.

$$Conv. Time = \frac{n + 2 + programmed\ sample\ clocks}{ATD\ clock\ frequency}$$

- ✓ Max. ATD clock frequency: 2 MHz. $\rightarrow ATD\ clock\ freq. = \frac{24\times10^6}{PRS+1} \times 0.5 = 2 \times 10^6 \rightarrow PRS = 5.$ `ATDnCTL4(4..0)=00101`
- ✓ Minimum Programmed sample clocks = 2. `ATDnCTL4(6..5)=00`
- ✓ n = 10. `ATDnCTL4(7)=0`

$$Min. Conv. Time = \frac{10 + 2 + 2}{2 \times 10^6} = 7us, ATDnCTL4 = 0x05$$